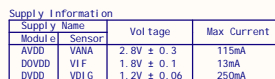


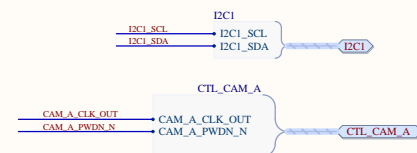
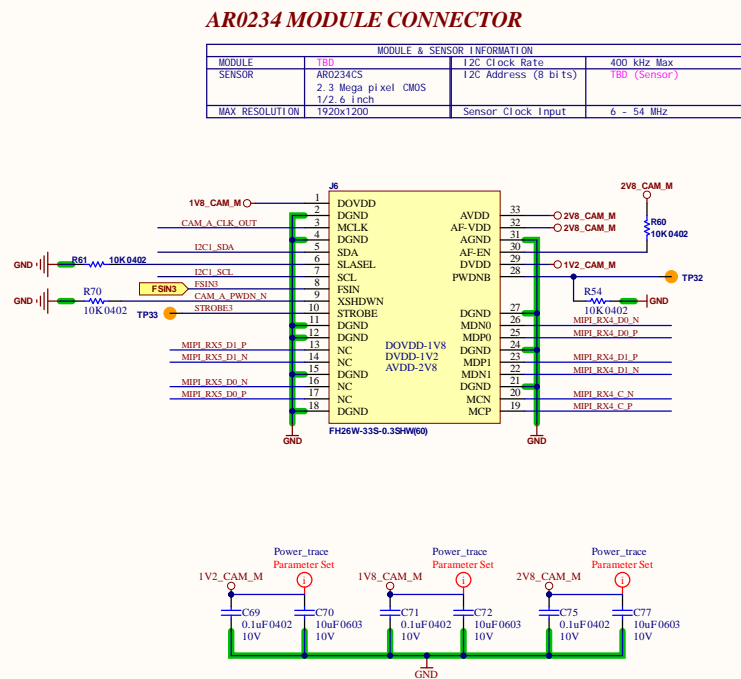
Project: BC2087
Current Revision: R1M1E1

BC2087 Revision History:

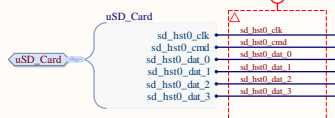
Date	Revision	Reason for Change	Changes Implemented
22/Aug/2022	Initial Release -> R0M0E0		
17/01/2023	R0M0E0 -> R1M0E1	<ul style="list-style-type: none">- Change the right camera to be connected to I2C3 not I2C0 as is at the moment.- Changed BNO INT and WAKE pins to IO42 and IO15 (MX) so that they are not on boot pins on KB.- PERST should be connected to IO- Right camera should have a sepearate reset line- Boot resistor for KB in wrong configuration- Expose UART for KB debugging- No space for THT UART pins- FSYNC should be PWM capable	<ul style="list-style-type: none">- Moved right camera to I2C3- Changed pins to IO42 and IO15 (MX)- Changed PCIE_PERST to IO39 (MX)- Added right camera reset line to IO43 (MX)- Depopulated R45- Added a header with I2C4/UART- Changed to SMD pins- Connected FSYNC to IO46 (MX) and IO14 (KB)



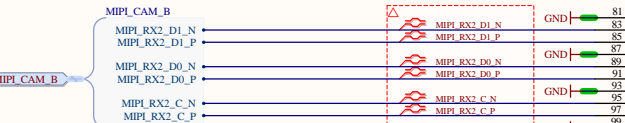
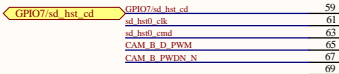
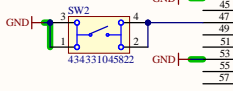
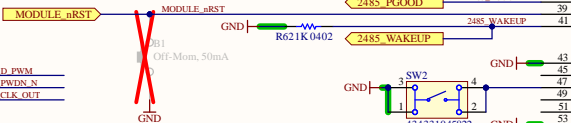
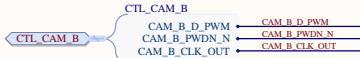
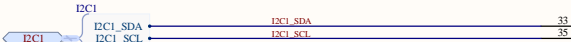
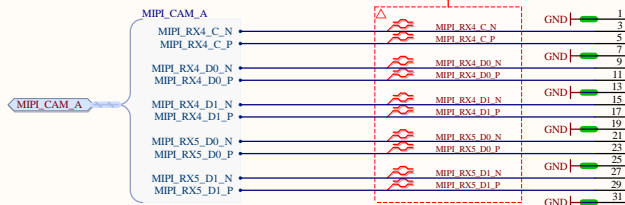
Note: It is still a limitation that the clock source for the cameras must be shared between CAMA/C and CAMB/D.



GND

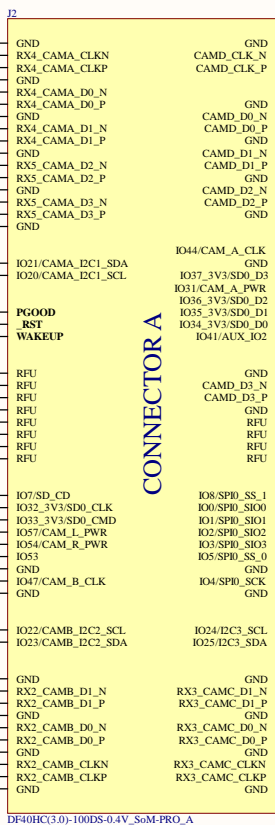


MIPI_CAMERA_A

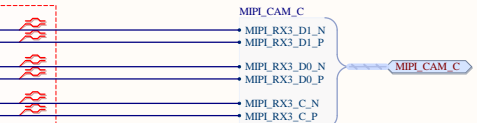
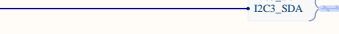
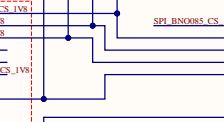
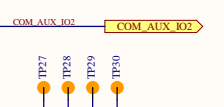
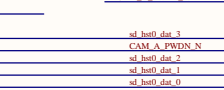
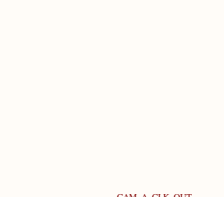
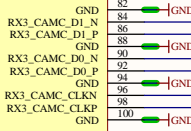
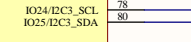
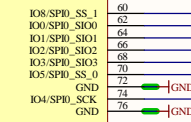
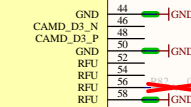
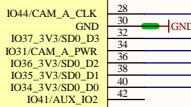
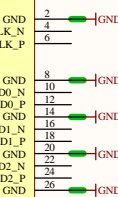


MIPI_CAMERA_B

CONNECTOR A



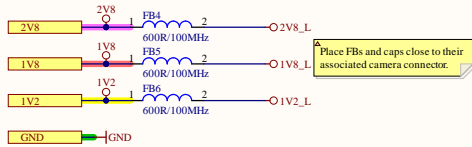
SDIO



MIPI_CAMERA_C

IMU SPI is length matched between connector and IMU. QSPI bus is length matched between connector and header pads.

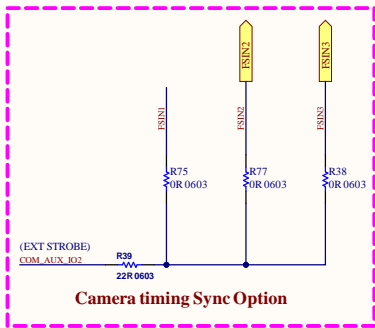
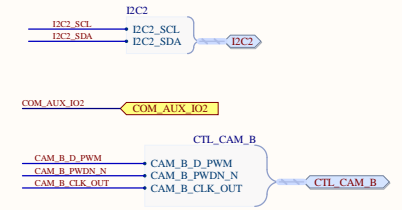
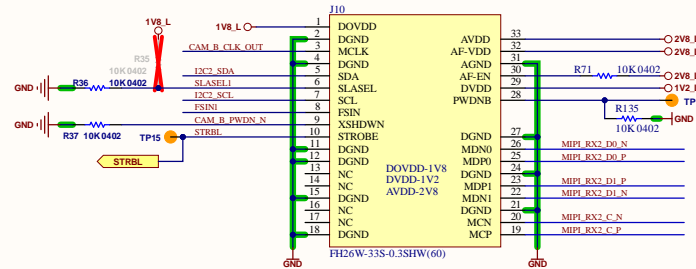
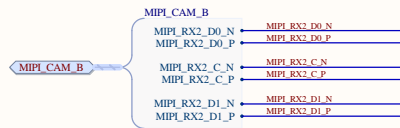
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Size: Tabloid	Number: D2088000	Revision: R1M1E1			
Date: 14/02/2023	Time: 16:57:58	Sheet 5 of 12			
Drawn by: Boris Chou / Blas Kvas					



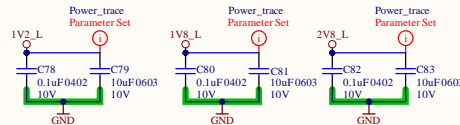
MODULE & SENSOR INFORMATION			
MODULE	TBD	I2C Clock Rate	400 kHz Max
SENSOR	AR0234CS	I2C Address (8 bits)	TBD (Sensor)
	2.3 Mega pixel CMOS		
MAX RESOLUTION	1920x1200	Sensor Clock Input	6 - 54 MHz

Supply Information			
Supply Name		Vol tage	Max Current
Module	Sensor		
AVDD	VANA	2.8V ± 0.3	115mA
DOVDD	V1F	1.8V ± 0.1	13mA
DVDD	VDIG	1.2V ± 0.06	250mA

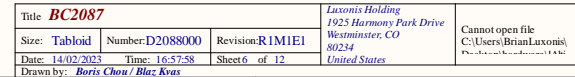
Mark "LEFT" on PCB
Place so that is the module's left camera.

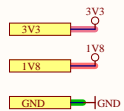


Need to check



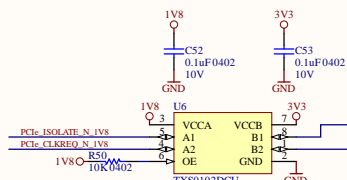
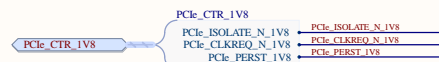
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Size: Tabloid	Number:D2088000	Revision:R1M1E1	Sheet 6 of 11		
Date: 14/02/2023	Time: 16:57:58	Drawn by: Boris Chou / Blas Kwas			



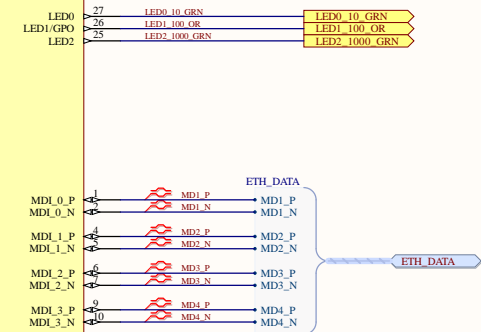
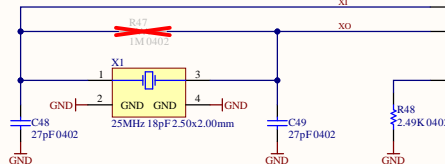
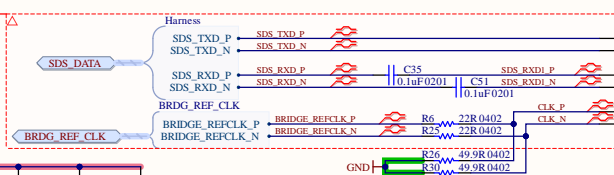


Power Sequence Requirements:
- 3.3V POR ramp must be: 0.5ms < t < 100ms
- All power inputs must be held >50ms at 0V between power cycles.
- 3.3V max power consumption is 202mA

Switching Regulator Layout:
- VDDREG >40mils
- REGOUT >60mils
- Place Lx and bulk C on the same layer as RTL8111HS
- No additional inductance or FBs
- Ceramic X5R caps or better



Drive PERST High to Enable PERST#
PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable.
Fundamental Reset for the PCIe Card

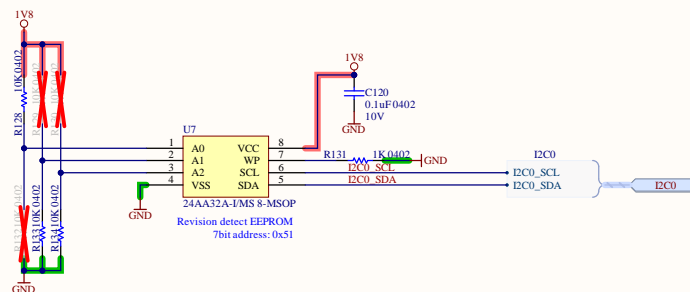


Schematic based on the reference design from the MV0247 PoE AOB reference design, with checking against the Realtek RTL8111HS reference design, layout guide, and datasheet.

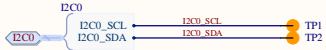
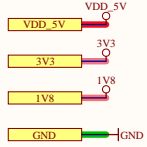
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Date: <i>14/02/2023</i>	Time: <i>16:57:58</i>	Sheet <i>7</i> of <i>12</i>			
Drawn by: <i>Boris Chou / Blas Kwas</i>					



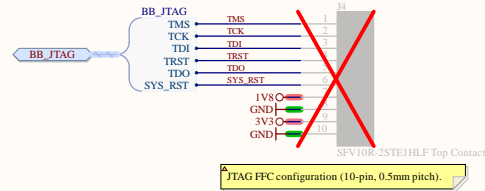
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Size: Tabloid	Number: D2088000	Revision: R1M1E1		
Date: 14/02/2023	Time: 16:57:58	Sheet 8 of 12		
Drawn by: Boris Chou / Blaz Kvas				



Title	<i>BC2087</i>		Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 <i>United States</i>	Cannot open file C:\Users\Brian\Luxonis\ Production\BorisChou\Bla
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Date:	14/02/2023	Time: 16:57:58	Sheet8 of 12	
Drawn by:	Boris Chou / Bla; Kvas			

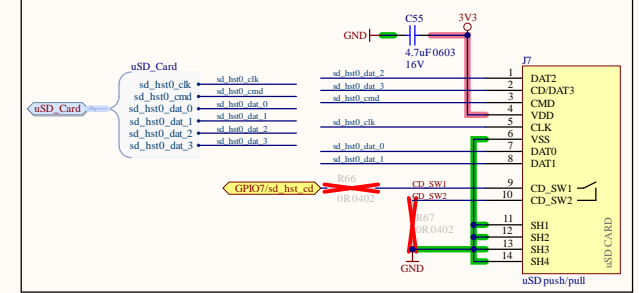


LED INDICATORS

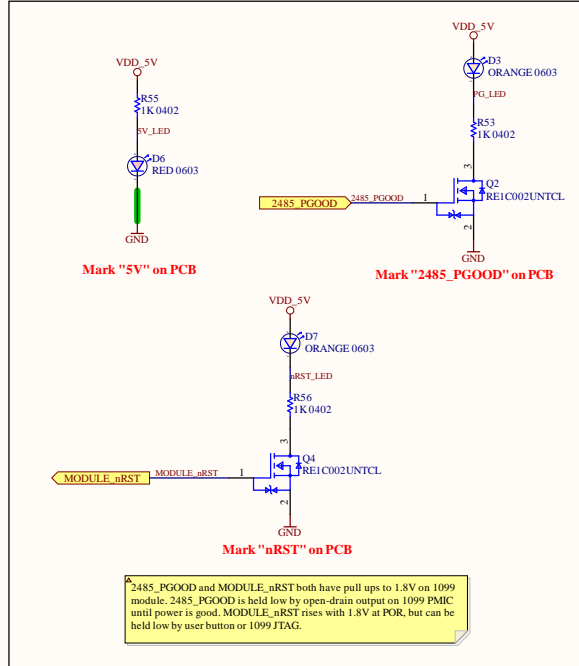


JTAG FPC configuration (10-pin, 0.5mm pitch).

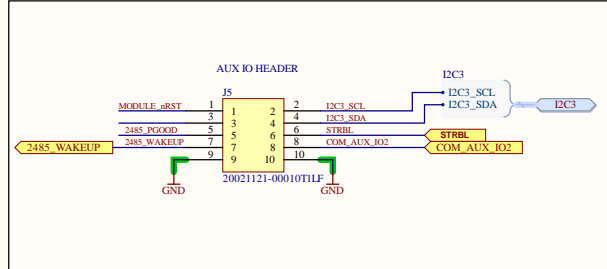
3.3V GPIO (uSD)



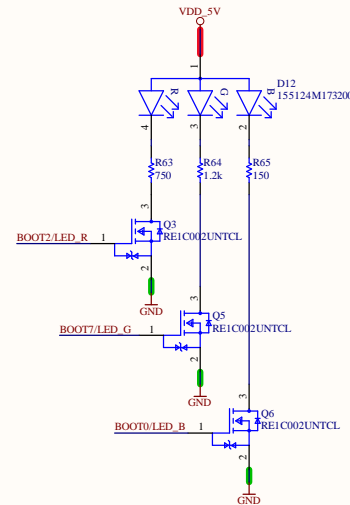
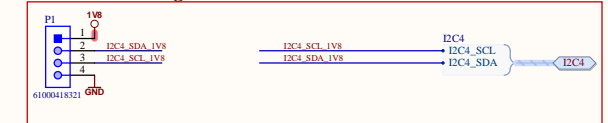
LED INDICATORS



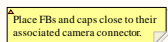
AUX IO HEADER



KB UART Debug

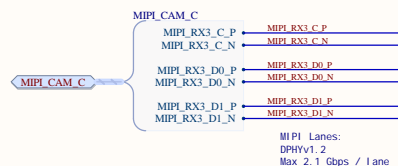


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Size: Tabloid	Number:D2088000	Revision:R1M1E1			
Date: 14/02/2023	Time: 16:57:58	Sheet9 of 12			
Drawn by: Boris Chou / Blas Kwas					

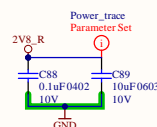
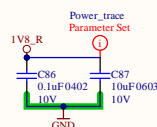
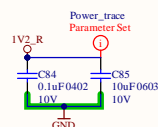
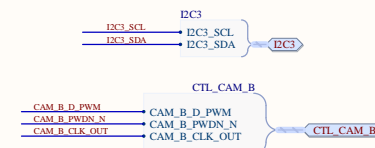
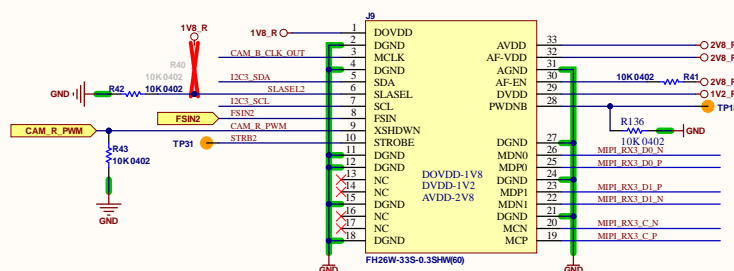


Supply Information

Supply Name		Voltage	Max Current
Module	Sensor		
AVDD	VANA	2.8V \pm 0.3	115mA
DOVDD	VIF	1.8V \pm 0.1	13mA
DVDD	VDIG	1.2V \pm 0.06	250mA



MIPI Lanes:
DPHYv1.2
Max 2.1 Gbps / Lane

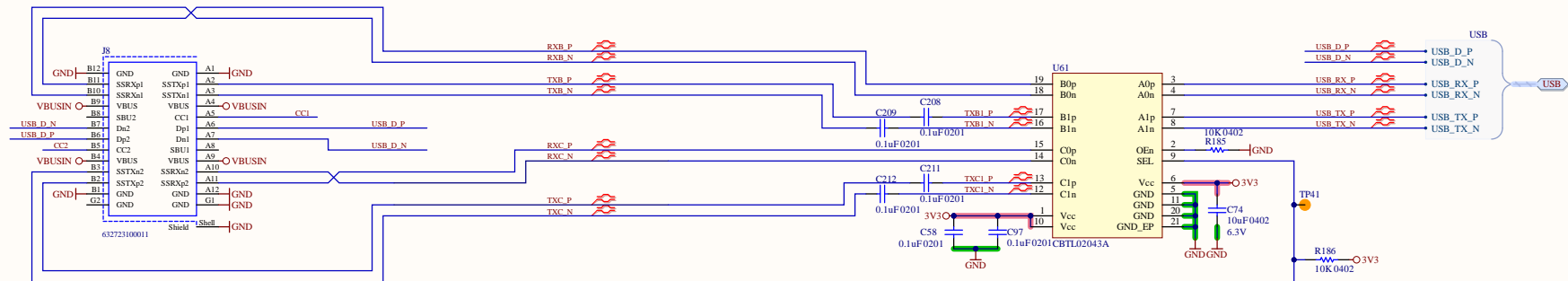
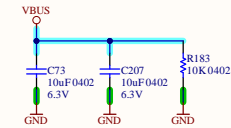
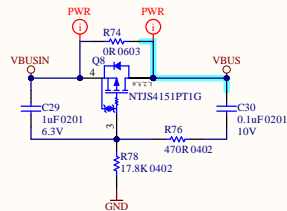


Because the stereo pair of OV9282 modules hard wired to CAM_B (below) no additional reset circuitry is required to account for different conditions. This means that "CAM1" (Left) is reset via CAM_PWDN, and "CAM2" (Right), is reset via CAM_PWM. This also means that the signal CAM_AUX_I01 is no longer required here, as that was only possible if the stereo pair were connected to CAM_C or CAM_D

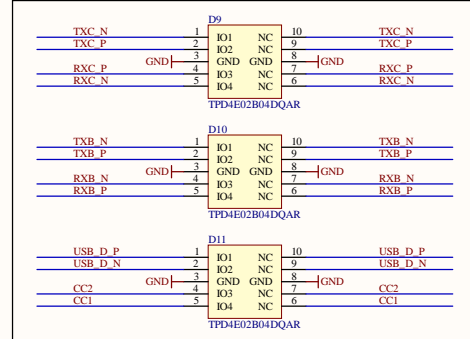
0V9282 sensor I2C address may be changed via I2C protocol. Therefore, in order to assign different I2C address to the sensors on the same I2C bus, one needs to hold the reset of all sensors except one and assign a unique I2C address to the active sensor. This routine should be applied for all sensors in the initialization routine.

CAM NO	CAMERA CONNECTOR			
	CAM_A	CAM_B	CAM_C	CAM_D
CAM 1	CAM_PWDN	CAM_PWDN	CAM_PWDN	CAM_PWDN
CAM 2	CAM_PWM	CAM_PWM	CAM_AUX I/O1	CAM_AUX I/O1

inrush current limiter

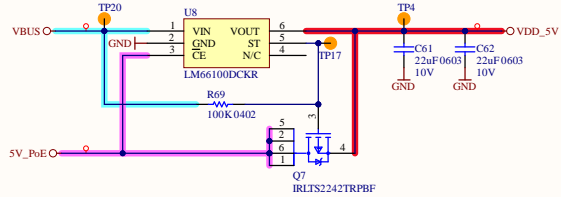
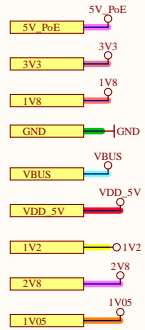


ESD PROTECTION

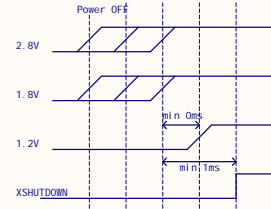


Title BC2087			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States	Cannot open file C:\Users\Brian\Luxonis\Documents\BC2087.dwg
Size: Tabloid	Number:D2088000	Revision:R1M1E1		
Date: 14/02/2023	Time: 16:57:58	Sheet 11 of 12		
Drawn by: Boris Chou / Blas Kwas				

POWER INPUT



AR0234 POWER REQUIREMENTS



Supply Information		Voltage	Max Current
Supply Name	Sensor		
DOVDD	VDD-I/O	1.8V	2.5mA
DVDD	VDD-D	1.2V	52mA
AVDD	VDD-A	2.8V	24mA

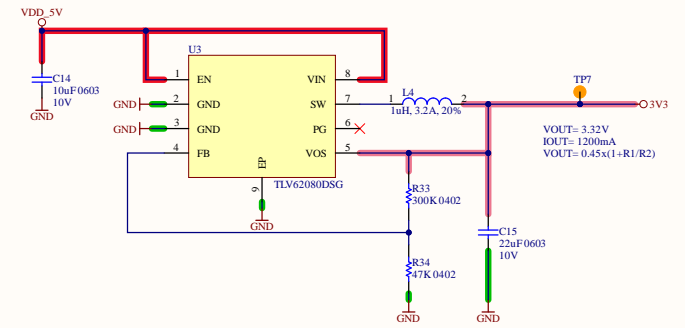
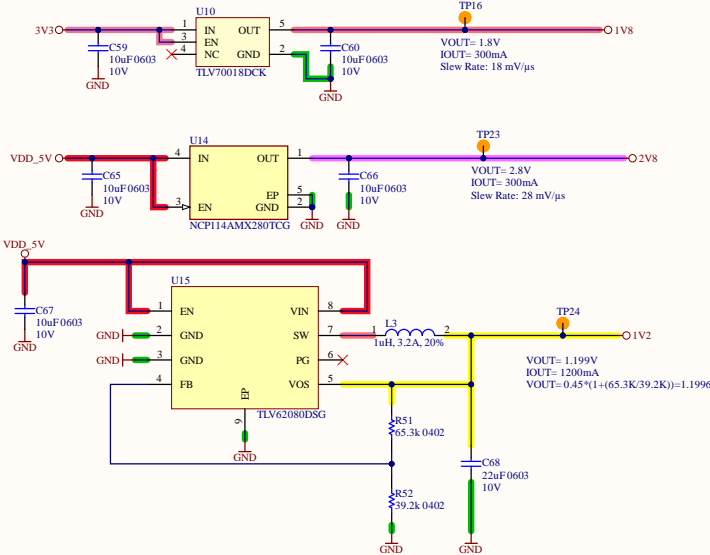
1. AVDD rising can occur before or after DOVDD rising as long as they are rising before XSHUTDOWN rising.
2. XSHUTDOWN is pulled up after AVDD and DOVDD are stable
3. DVDD rises after DOVDD, but before XSHUTDOWN is pulled high

POWER SEQUENCING REQUIREMENTS:

The BW2099 module handles it's own power sequencing on-board. (TBC)

The camera modules have their own power sequencing requirements. The OV9282 have requirements for sequencing, and the IMX378 has a max slew rate requirement. See above.

POWER SUPPLIES FOR CAMERA MODULES



Title BC2087			Luxonis Holding 1925 Harmony Park Drive Westminster, CO 80234 United States	Cannot open file C:\Users\BrianLuxonis\Documents\BC2087.dwg
Size: Tabloid	Number: D2088000	Revision: R1M1E1		
Date: 14/02/2023	Time: 16:57:58	Sheet 12 of 12		
Drawn by: Boris Chou / Blas Kwas				